2 bit adder carry and sum logic circuits at 19 GHz clock frequency in Transferred Substrate HBT technology.

T. Mathew, S. Jaganathan*, D. Scott, S. Krishnan, Y. Wei, M. Urteaga, M. J. W. Rodwell, S. Long
Department of ECE,
University of California Santa Barbara, CA 93106
Tel.: (805) 893-8044 / Fax: (805) 893-3262E-mail: **thomas@goodness.ece.ucsb.edu**

We report carry and sum circuits for a 2 bit adder. The 2 bit adders are designed to be cascaded into a pipelined 2N bit adder-accumulator. The ICs clock at a maximum of 19GHz and were fabricated in InAlAs/InGaAs transferred substrate HBT technology [2]. To obtain high clock rates in a design with multiple gate delays we have employed a novel merged AND-OR logic structure using 4 level series gated current steering logic. Further, this logic is merged with the synchronizing latch circuit so as to minimize the overall gate delay. The 2 bit carry generation circuit (Fig. 1) has 250 transistors, a maximum clock frequency of 19GHz, and dissipates 1.2W. The sum logic circuit of a full adder was realized as a 3 level series gated ECL XOR gate, as shown in Fig 2. This circuit has a maximum clocking frequency of 24 GHz, has 150 transistors and dissipates 750mW.

Pipelined adder-accumulators are used as phase accumulators in direct digital frequency synthesis (DDFS) systems that require high clock frequency [1,3] The maximum clock frequency is limited by the delay in the carry logic circuitry [1]. Conventional approaches generate the carry logic C_1 ($C_1 = A_0B_0 + A_0C_0 + B_0C_0$) as 3 two input AND gates followed by a 3 input OR gate. Here we demonstrate a 3 input series gated ECL logic gate that generates the carry bit. Simulations indicate a 40% improvement in clock rate can be achieved by this approach. Pipelined adders require regular latching for synchronization [1]. The ICs reported here have the master-slave latch merged with the logic stage by gating the logic by the clock, resulting in a 4 level series gated structure (Fig. 1). This provides an additional improvement of about 40% in clocking speed compared to latching the output using a master slave latch.

The circuits were fabricated in InAlAs/InGaAs transferred substrate HBT technology [2]. A minimum device geometry of $3.0\times 1.0\mu m$ emitter and $3.0\times 2.0\mu m$ collector, was used with measured f_t = 140GHz, f_{max} = 160GHz, current gain β = 5-10, at $J_e=1\times10^5$ A/cm^2 and Vce=1.0V. The low current gain β and low transistor speed was due to an error in base epitaxial growth. For high frequency testing both the carry and the sum logic circuit were configured as frequency dividers by feeding back the output of the adder as one of the adder inputs (Fig. 1 and Fig. 2). The maximum clock frequency is then measured. Given HBT performance normally achieved in this process (β=50, f_t = 220GHz, f_{max} = 300GHz), simulations predict a clock rate of above 40GHz. ICs with correct MBE layers have been processed and are being tested.

Acknowledgements: This was supported by the Office of Naval Research (ONR) under contract titled: 100 GHz logic technology, ONR 97: N00014-98-1-0068.

References

[1] Charles. G. Ekroot et.al., A GaAs 4 bit adder-accumulator circuit for direct digital synthesis, IEEE, Journal of solid state circuits, Vol 23, No:2, April 1988, pp 573-579.
[2] Q. Lee et al., 11th International Conference on Indium Phosphide and Related Materials, 16-20 May 1999, Davos, pp. 175-178
[3] V. Manassewitsch, Frequency synthesizers theory and design, New York: Wiley-interscience, 1980, pp 37-43.

* GTRAN Inc, Westlake village, CA 91362

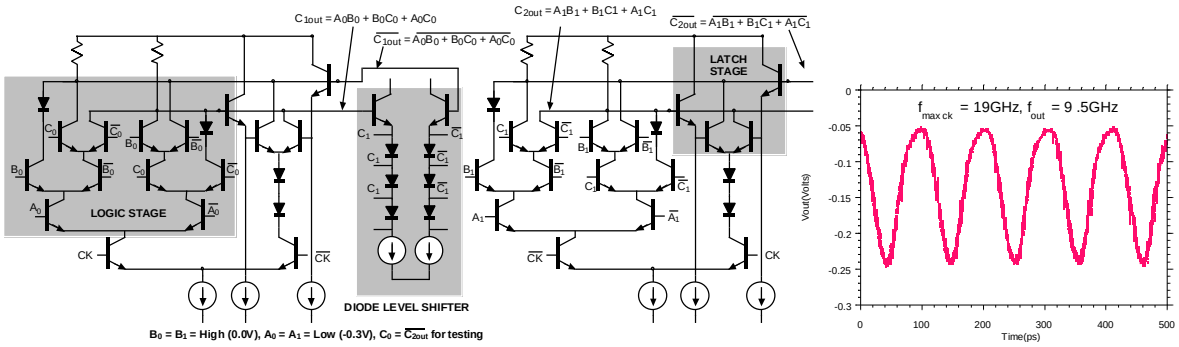

Fig. 1: Two bit carry logic circuit showing the carry generation and the clocking approach. For testing purposes the circuit was configured as a frequency divider. Output waveform is shown at 19GHz clock.

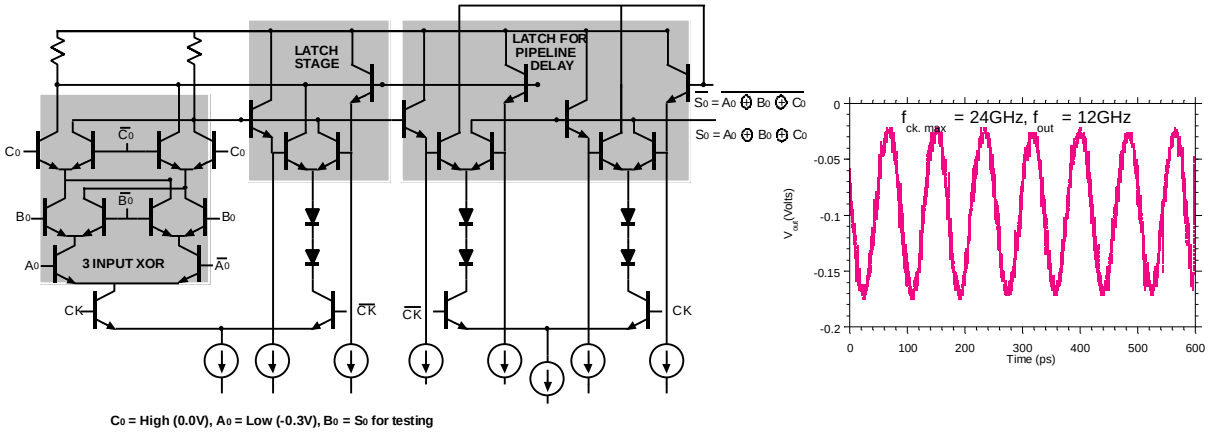

Fig. 2: Sum circuit for sum logic generation. The IC is again configured as a frequency divider for testing. The output waveform is shown for 24GHz clock frequency

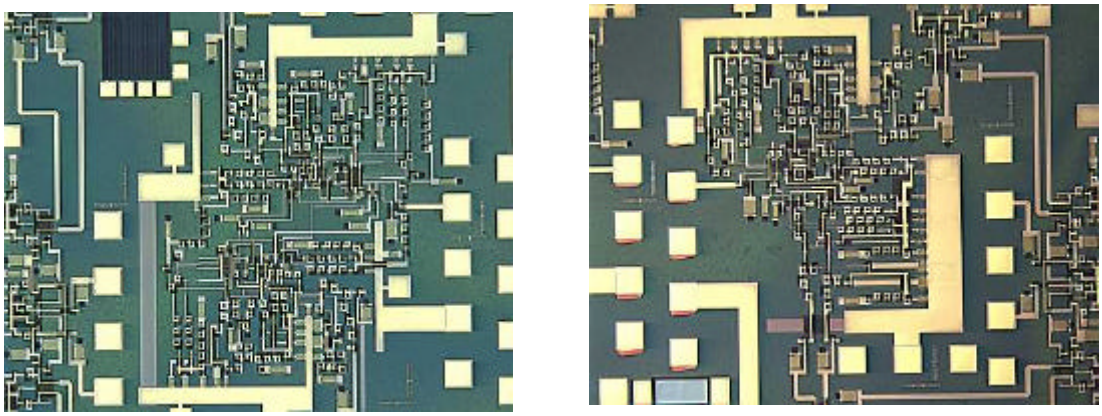

Fig. 3: Chip photograph of the 2 bit carry logic circuit on the left and 1 bit sum logic circuit on the right.